

EXPRESS MAIL MAILING LABEL

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Signature

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

MARK S. FUSELIER
DERICK J. WRISTERS
ANDY C. WEI

Group Art Unit: Unknown

Examiner: Unknown

Serial No.: Unknown

Attorney Docket: 2000.092182/TT5077D

Filed: Concurrently Herewith

Customer No.: 23720

For: SEMICONDUCTOR DEVICE FORMED
OVER A MULTIPLE THICKNESS
BURIED OXIDE LAYER, AND
METHODS OF MAKING SAME

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with the duty of disclosure under 37 C.F.R. § 1.56, it is respectfully requested that this Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 be considered by the Examiner and made of record. Copies of the listed documents required by 37 C.F.R. § 1.98(a)(2) are enclosed for the convenience of the Examiner.

In accordance with 37 C.F.R §§ 1.97(g),(h), this Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be

an admission that the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

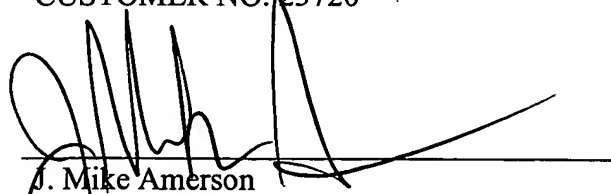
This application is a divisional application of Serial No. 10/109,096, filed March 28, 2002, and is relied upon for an earlier filing date under 35 U.S.C. § 120. In accordance with Rule 37 C.F.R. § 1.98(d), only copies of those documents not previously cited and submitted to the Patent and Trademark Office in prior application Serial No. 10/109,096 are enclosed for the convenience of the Examiner

The present Information Disclosure Statement is being filed within three months of the filing date of this patent application or prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Information Disclosure Statement; however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Director is hereby authorized to deduct said fees from Williams, Morgan & Amerson, P.C., Deposit Account No. 50-0786/2000.092182.

Applicants respectfully request that the listed documents be made of record in the present case.

Respectfully submitted,

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Date: April 8, 2004

ATTORNEY FOR APPLICANTS

Form PTO-1449 (modified)		Atty. Docket No. 2000.092182/TT5077	Serial No. Unknown
List of Patents and Publications for Applicant's INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		Applicant Mark S. Fuselier, Derick J. Wristers and Andy C. Wei	
		Filing Date: Concurrently Herewith	Group: Unknown
U.S. Patent Documents See Page 1	Foreign Patent Documents See Page 1	Other Art See Page 1	

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date of App.
	A1	5,482,871	01-1996	Pollack	438	151	
	A2	5,926,703	07-1999	Yamaguchi <i>et al.</i>	438	163	
	A3	5,950,094	09-1999	Lin <i>et al.</i>	438	409	
	A4	6,069,054	05-2000	Choi	438	423	
	A5	6,180,487	01-2001	Lin	438	407	
	A6	6,204,546	03-2001	Roitman <i>et al.</i>	257	506	
	A7	6,232,163	05-2001	Voldman <i>et al.</i>	438	212	
	A8	6,352,882	03-2002	Assaderaghi <i>et al.</i>	438	155	
	A9	6,407,428	06-2002	Krishnan <i>et al.</i>	257	374	
	A10	6,531,375	03-2003	Giewont <i>et al.</i>	438	407	

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1	0 687 002 A2	12/13/95	Europe	H01L	21/762	Yes
	B2	WO 00/48245	8/17/00	PCT	H01L	21/762	Yes

Other Art (Including Author, Title, Date Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C1	Baine <i>et al.</i> , "Back Gate Effects in N-Channel Monocrystalline Silicon Devices-on-Glass and Their Suppression by Boron Ion Implantation," <i>Mat. Res. Soc. Symp. Proc.</i> , 558:369-74, 2000
	C2	Chang <i>et al.</i> , "Efficacy of Air in Reducing the Kink Effect on Floating-Body NFD/SOI CMOS," <i>Proc. 1998 IEEE Int'l SOI Conf.</i> , pp. 155-56, 1998
	C3	Ko <i>et al.</i> , "Suppression of Floating Body Effect with SIGE Source Structure for Fully Depleted SOI MOSFET's," <i>Electrochem. Soc. Proc.</i> , 2001-3:239-44, 2001
	C4	Leung <i>et al.</i> , "High Voltage, High Speed Lateral IGBT in Thin SOI for Power IC," <i>Proc. 1996 IEEE Int'l SOI Conf.</i> , pp. 132-133, 1996

EXAMINER:

DATE CONSIDERED:

EXAMINER: INITIAL IF REFERENCE CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED. INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.